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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,188	09/28/2005	Richard John Payman	040857/291463	4571
826	7590	07/13/2007	EXAMINER	
ALSTON & BIRD LLP			DEB, ANJAN K	
BANK OF AMERICA PLAZA			ART UNIT	
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CHARLOTTE, NC 28280-4000			2858	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,188	PAYMAN, RICHARD JOHN	
	Examiner	Art Unit	
	Anjan K. Deb	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 May 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 10, 19-36, 38 and 39 is/are pending in the application.
- 4a) Of the above claim(s) 1, 19-27 and 36 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10, 28-35, 38 and 39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) 1, 10, 19-36, 38 and 39 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04/28/2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>04/28/2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims of Group II Claims 10, 28-36, 38 and 39 in the reply filed on 05/25/2007 is acknowledged. However, it appears that claim 36 depends from non-elected claim 19 and has been withdrawn from further consideration.

Examiner regrets the error in the Grouping of claims in the Election/Restriction requirement of claims in the office action filed 04/27/2007, which is hereby corrected to include the claims 1,19-27 and 36 in the invention of Group I, and the claims 10, 28-35, 38 and 39 in the invention of Group II.

Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 1 and 19-27, 36 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Group I invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 05/25/2007.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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3. Claims 10, 28-35, 38 and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Laing et al. (US 5,399,975).

Re claim 10, Laing et al. disclosed method of testing the continuity of a connection between an integrated circuit pin 15 (Fig. 1) and a circuit board 7 where the integrated circuit pin 15 is connected to a plurality of integrated circuit pins 11,13 forming a first group, the method comprising the steps of: identifying a second group of integrated circuit pins (inherent to second device 9)(Fig. 4) having electrical properties relatable to the first group; applying one or more first test signals to the first group of pins (column 3 line 24) and measuring one or more respective first voltage differences occurring between the first group of pins and a reference voltage; applying one or more second test signals to the second group of pins (column 3 lines 33-38) and measuring one or more respective second voltage differences (change in output voltage) (column 4 line 24) occurring between the second group of pins and a reference voltage; and on the basis of measurements extracting and comparing a non-linear characteristic (exponentially) (Fig. 6 iv) (column 4 line 23) of the first and second group of pins to obtain a measure of said continuity (column 4 lines 26-31).

Re claims 28, 32 Laing et al. disclosed all of the claimed limitations as set forth above including applying M and N test signals (through matrix of relays) to first and second group of pins (column 3 lines 14-17) wherein the disclosed M and N test signals (provided by matrix of relays) are substantially identical current waveforms (Fig. 6, i,ii,iii).

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Re claim 29, 30 Laing et al. disclosed first and second device 9 (Fig. 4). The two devices identified by the same numeral 9 in the figure has been broadly considered to be the same type of device having similar function and technology and comprising the same number of device pins.

Re claims 31, 33, Laing et al. disclosed M and N test signals (matrix of relays) are DC signals (5V or 0V) of switchable (transistor switches) value (column 3 lines 14-17) and determining a faulty connection if the difference in voltage (V_{out}) exceeds a threshold (column 4 lines 29-31)(Fig. 6 iv).

Re claim 34, Laing et al. disclosed M and N test signals (matrix of relays) comprise an AC component superimposed on a DC component (Fig. 6, iii, iv) and the magnitude of harmonic components of the voltage differences are compared and a faulty connection is indicated if the difference in harmonic components exceeds a threshold value (column 4 line 14, 23-25, 29-31). AC component shown Fig. 6 is broadly interpreted as the harmonic components.

Re claim 35, Laing et al. disclosed non-linear characteristics V_{out} (Fig. 6 iv) is performed directly by extracting a non-linear characteristic based on forming a difference between the first voltage difference and the second voltage difference (change in the output voltage) (column 4 line 14, 23-25, 29-31).

Re claim 38, Laing et al. disclosed all of the claimed limitations as set forth above including wherein the first and second testers 5(plurality of inductive probes)(Fig. 2,5) are

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adapted such that the test signals applied to the groups of pins (11,15,13) comprise discrete time samples of a sinusoidal or other waveform (Fig. 6 i) having little or zero low-order harmonic content and the testers are further adapted to use the measured voltage differences as discrete samples in reconstructing the response to a sinusoidal or other waveform having little or zero harmonic content input for harmonic analysis (Fig. 6, ii,iii,iv).

Re claim 39, Laing et al. disclosed test signal generator (ATE SYSTEM 1)) (Fig. 1) for generating a probe current which is injected via a further device connection (ICT FIXTURE 3) into a selected integrated circuit 9, and wherein the continuity test is repeated and the selected integrated circuit is indicated as having an unacceptable connection if the non-linear characteristic (Fig. 6 iv) varies by more than a first predetermined threshold (THRESHOLD VOLTAGE), or is indicated as having an acceptable connection if the non-linear characteristic varies by more than a second predetermined threshold of opposite sign to the first predetermined threshold (Fig. 6 iv).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Stine et al. (US 2005/0122123 A1) disclosed test structure for continuity testing (open and short defects) of semiconductor device by applying test voltage between nodes (Fig. 3, 4A, 4B).

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Long (US 7,109,736 B2) disclosed system for measuring signal path resistance between nodes 21A, 21N of integrated circuits 12 by applying test current, measuring voltage and calculating the resistance of signal path (Fig. 3).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Anjan K. Deb whose telephone number is 571-272-2228. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew H. Hirshfeld can be reached at (571) 272-2168.



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Primary Patent Examiner

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7/5/07

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